

An Output-Capacitor-Free Adaptively Biased LDO Regulator with Robust Frequency Compensation in 0.13 μ m CMOS for SoC Application

Conference Paper

Author(s):

Han, Xu; Burger, Thomas; Huang, Qiuting

Publication date:

2016

Permanent link:

<https://doi.org/10.3929/ethz-a-010810287>

Rights / license:

[In Copyright - Non-Commercial Use Permitted](#)

An Output-Capacitor-Free Adaptively Biased LDO Regulator with Robust Frequency Compensation in $0.13\mu\text{m}$ CMOS for SoC Application

Xu Han
Integrated Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
Email: xhan@iis.ee.ethz.ch

Thomas Burger
Integrated Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
Email: burger@iis.ee.ethz.ch

Qiuting Huang
Integrated Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
Email: huang@iis.ee.ethz.ch

Abstract—This paper presents a fast-response low-dropout (LDO) regulator using a current feedback loop to realize an adaptive biasing error amplifier. With the proposed current feedback loop, the LDO regulator achieves 34dB higher loop gain, 46% faster transient response, and about 12dB higher power supply rejection above 1MHz than the one with fixed biasing. The adaptively-biased LDO regulator is compensated by a simple Miller compensation using adaptive nulling resistor (SMCANR). The proposed compensation network can realize robust frequency compensation and reduce voltage spikes during load transients. An expanded stability analysis using the Routh-Hurwitz criterion gives designers additional freedom for a stable design. Designed in a $0.13\mu\text{m}$ CMOS technology for a minimum dropout voltage of 200mV, the LDO regulator supplies 1.2V at 98.2% current efficiency and 10mA load current.

I. INTRODUCTION

Power management is a very important topic in portable electronics, such as cellular phones, tablets, or other personal digital assistants. Generally, advanced devices have become highly integrated containing only few ICs that constitute whole Systems-on-Chip (SoC). In such SoC, various converter types are required for power management. Among these converters, low-dropout (LDO) regulators are widely used to provide clean voltage supplies with low ripple for noise-sensitive and/or RF blocks. For hand-held applications, external components such as output capacitors should be minimized to reduce the printed-circuit-board layout space and to speed up the manufacturing process. Hence, output-capacitor-free LDO regulators are preferred in recent years [3]- [7].

Advanced compensation techniques such as simple Miller compensation using nulling resistor [1], adaptive zero compensation [2], and damping-factor-control frequency compensation [3] were proposed to improve loop stability with reasonable silicon estate in recent years. Also, voltage-spike detection [4] and slew-rate enhancement [5] were developed to enhance transient response. [7] shows high loop gain is necessary for a higher PSR and lower output impedance. In [3], we can see the low frequency loop gain drop substantially at heavy load currents. The adoption of high I_{bias} to enhance the low frequency loop gain is important, which improves PSR and reduces both load and line ripple. However, the high- and fixed- I_{bias} strategy limits current efficiency, especially

at light load. It is difficult to extend the loop gain bandwidth product while maintaining high current efficiency with fixed biasing current. In recent years, the adaptively biased LDO (ABLDO) regulator topology [7]- [9] achieved this desirable feature without significant degradation of the current efficiency. The biasing current is composed of a fixed biasing current I_{bias} and an adaptive feedback current I_{AB} . At heavy load, the feedback current I_{AB} increases the error amplifier biasing current, which extends the loop bandwidth; at light loads, the low fixed current I_{bias} maintains high current efficiency. The loop stability is a critical issue, especially when the adaptive biasing is employed. Most designers prefer to analyze stability in time domain, because of the lack of a good frequency analysis method.

This paper proposes an adaptively-biased LDO regulator using simple Miller compensation with an adaptive nulling resistor (SMCANR). The proposed LDO regulator achieves both extended loop bandwidth and high current efficiency. The SMCANR compensation network helps to realize a robust frequency compensation in a wide operating range. An extended stability analysis is provided in this work, which helps designers to achieve a stable circuit operation with frequency domain analysis. Section II presents the proposed LDO regulator theoretical analysis with a detailed discussion on the stability in frequency domain. Section III shows the simulation results for a $0.13\mu\text{m}$ CMOS implementation, and Section IV provides the conclusions.

II. PROPOSED ADAPTIVE BIASING LDO REGULATOR

Fig. 1 shows a simplified schematic of the proposed adaptively-biased LDO (ABLDO) regulator. The ABLDO regulator is partitioned into three parts: the main feedback loop (MFL), the adaptive biasing feedback loop (ABL), and the SMCANR compensation network. The load capacitor C_L is 100pF for this design, and the load current ranges from 0 to 10mA. The pass transistor M_p is kept in saturation region across the whole operating range. The feedback voltage V_{MF} is the scaled output voltage by the resistive divider (R_{F1} , R_{F2}) at low frequencies and the capacitor divider of C_F and the parasitic capacitance present at the gate node of M_1 at high frequencies. In this work, we use a class-A amplifier topology biased with a fixed biasing current I_{bias} and an

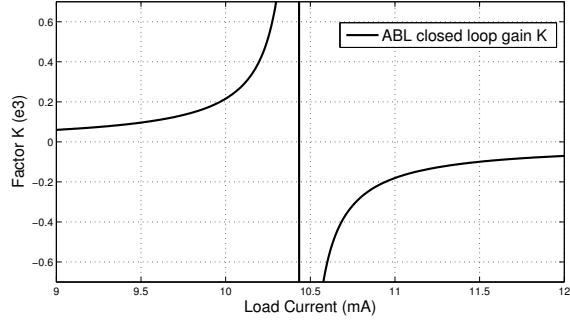


Fig. 3. ABL closed loop gain K vs. I_{load} .

that will show how closed loop system stability can also be reached for $K < 0$. Since the MFL is a negative voltage feedback system, the system closed loop transfer function is

$$T(s) = \frac{G(s)}{1 + G(s)\beta} \quad (8)$$

The closed loop poles are the solutions of

$$a_3s^3 + a_2s^2 + (a_1 + A_{DC}b_1)s + 1 + A_{DC} = 0 \quad (9)$$

The system is stable only when all closed loop poles have negative real part. To derive conditions for this to be fulfilled, we use the Routh-Hurwitz criterion [10], which is widely used in control engineering for the stability analysis of closed loop systems.

$$\begin{array}{ccc} s^3 & a_3 & a_1 + b_1A_{DC} \\ s^2 & a_2 & 1 + A_{DC} \\ s^1 & c_1 & \\ s^0 & 1 + A_{DC} & \end{array} \quad (10)$$

where

$$c_1 = \frac{a_2(a_1 + b_1A_{DC}) - a_3(1 + A_{DC})}{a_2} \quad (11)$$

$$\approx r_{o3}C_{AB}K + (R'_M C_M - \frac{R_o C_L R'_M C_M}{R_o C_L + R'_M C_M})A_{DC}$$

In terms of the Routh-Hurwitz criterion, all the poles have negative real part only if all the components in the second column of Eq. 10 have the same sign. b_1 is positive by a well compensated design. a_3 , a_2 and c_1 have the same sign as K since $R'_M C_M > (R'_M C_M) \parallel (R_o C_L)$. In order to fulfill the Routh-Hurwitz criterion, also $sign(K) = sign(1 + A_{DC})$ must be fulfilled. This is always fulfilled if $K > 0$ (left side in Fig. 3) and can be translated to $|A_{DC}| > 1$ and further to

$$|K| > \frac{1}{g_{m1}g_{mp}r_{o3}R_o\beta}, \quad K < 0 \quad (12)$$

which can be made valid over the entire range of LDO operation by appropriate design (right side in Fig. 3). The stability vs. K is demonstrated in Fig. 4 which contains the open loop frequency response for the cases $I_{load} = 10\text{mA}$, $K > 0$ and $I_{load} = 11\text{mA}$, $K < 0$ and the corresponding time domain transient behavior for both cases and a step from $I_{load} = 0$ to $I_{load} = 10$ or 11mA , respectively.

As shown in Eq. 1, the open loop transfer function is

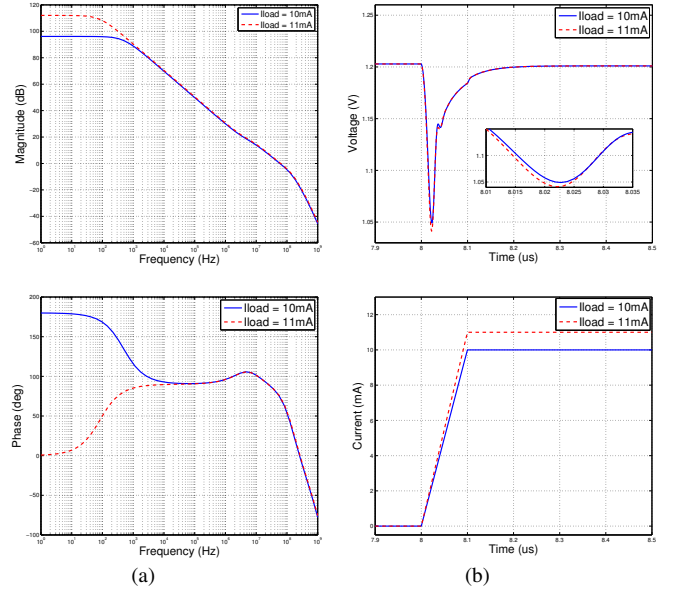


Fig. 4. $I_{load} = 10\text{mA}$ and 11mA (a) MFL frequency responses, (b) Output time response.

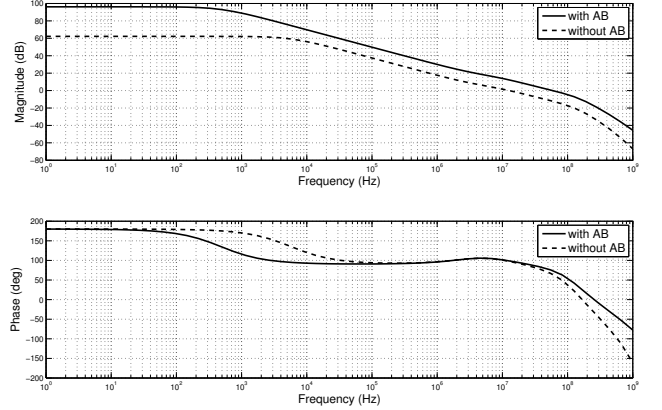


Fig. 5. MFL frequency responses at $I_{load} = 10\text{mA}$ with and without adaptive biasing.

a third order system with a LHP zero, and the dominant pole is created at the output of the OTA. Pole-splitting helps to achieve sufficient phase margin. For the maximum phase margin, the first non-dominant pole should be canceled by the LHP zero [1]. This condition is fulfilled when

$$R'_M = \frac{1}{g_{mp}}(1 + \frac{C_L}{C_M}) \quad (13)$$

The right part of the equation is inversely proportional g_{mp} and therefore shows an inverse relation to the load current as well. For a fixed nulling resistor, the maximum phase margin cannot be achieved in a wide operating range. While, the adoption of the proposed adaptive nulling resistor R'_M tracking $1/g_{mp}$ helps to achieve sufficient phase margin across the whole operating range.

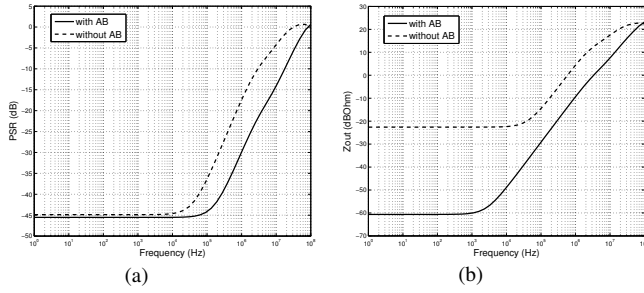


Fig. 6. The two LDO regulators at $I_{load} = 10\text{mA}$ (a) PSR, (b) Output impedance

III. SIMULATION RESULTS

The proposed ABLDO regulator is designed in a $0.13\mu\text{m}$ CMOS technology for an input voltage of 1.4-1.5V, a regulated output voltage of 1.2V, and a load current range from 0 to 10mA. The fixed biasing current of the error amplifier is $20\mu\text{A}$, and the feedback ratios B and D have been chosen as 100 and 1, respectively. At light load $I_{load} = 100\mu\text{A}$, the current efficiency is 82.7%, and at heavy load $I_{load} = 10\text{mA}$, the current efficiency increases to 98.2%.

At full load of 10mA, the LDO regulator with ABL disabled has a phase margin $PM = 98^\circ$, gain margin $GM = 24\text{dB}$, open loop gain $Gain = 62\text{dB}$, and unity gain bandwidth $UGBW = 13\text{MHz}$; while, the proposed ABLDO regulator with ABL has a $PM = 74^\circ$, $GM = 17.5\text{dB}$, $Gain = 96.1\text{dB}$, and $UGBW = 59\text{MHz}$, as shown in Fig. 5. The ABL feedback increases the open loop gain and extends the gain bandwidth substantially. This helps to increase PSR from -17.4dB to -29.9dB at 1MHz, and reduces Z_{out} from $-22.6\text{dB}\Omega$ to $-60.6\text{dB}\Omega$ at full load and low frequency, as shown in Fig. 6.

The SMCANR compensation network also contributes to a better transient response. As illustrated in Fig. 7 (a), when the load current changes from 1mA to 10mA in 100ns, the output voltage ripple with ABL is only 30.3mV and settling time to 10% of the final step level is $0.205\mu\text{s}$, instead of 38.2mV and $0.377\mu\text{s}$ without ABL. Fig. 7 (b) shows the settling behavior of line regulation. When the input voltage steps up from 1.4V to 1.5V in 100ns, the voltage ripple with ABL is 4.8mV and settling time to 10% of the final step level is $0.243\mu\text{s}$, instead of 20.4mV and $0.340\mu\text{s}$ without ABL; when the input voltage steps down from 1.5V to 1.4V in 100ns, the voltage ripple with ABL is 4.7mV and settling time is $0.238\mu\text{s}$, instead of 20.1mV and $0.393\mu\text{s}$ without ABL.

IV. CONCLUSION

This paper investigates an adaptively-biased LDO regulator with SMCANR compensation network. The adoption of the SMCANR compensation network helps to achieve a faster load and line transient response with reduced voltage ripple, and also to realize a robust compensation under a wide range of load current. The proposed ABLDO regulator extends the loop gain bandwidth significantly, leads to a better PSR and lower Z_{out} , and maintains a high current efficiency over the specified load current range. An extended stability analysis for the LDO regulator is provided that increases the range of allowable feedback current to previous work [7]. The use of

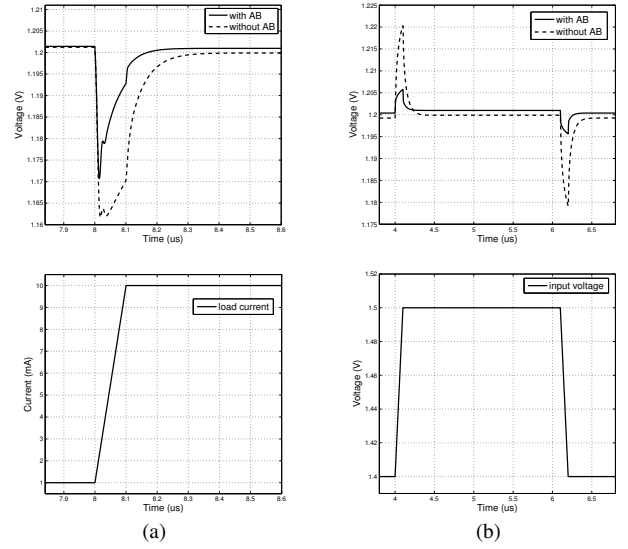


Fig. 7. Transient responses (a) Load transient response, (b) Line transient response.

Routh-Hurwitz criterion helps to derive the stability condition for the present ABLDO regulators even when the ABL open loop gain is above 1. The theoretical analysis has been verified by extensive simulations.

REFERENCES

- [1] J. Rogin, "Direct-conversion receiver design for wideband cellular communications", *PdD thesis, Eidgenössische Technische Hochschule ETH Zürich*, Nr. 15506, 2004, pp. 137-140.
- [2] H. C. Yang, M. H. Huang, and K. H. Chen, "High-PSR-bandwidth capacitor-free LDO regulator with $50\mu\text{A}$ minimized load current requirement for achieving high efficiency at light loads," *WSEAS Trans. Circuits Syst.*, vol. 7, no. 5, pp. 428-437, May 2008.
- [3] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691-1702, Oct. 2003.
- [4] P. Y. Or and K. N. Leung, "An output-capacitorless low-dropout regulator with direct voltage-spike detection," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458-466, Feb. 2010.
- [5] E. N. Y. Ho and P. K. T. Mok, "A capacitor-less CMOS active feedback low-dropout regulator with slew-rate enhancement for portable on-chip application," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 2, pp. 80-84, Feb. 2010.
- [6] Y. I. Kim and S. S. Lee, "A capacitorless LDO regulator with fast feedback technique and low-quiescent current error amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 6, pp. 326-330, Jun. 2013.
- [7] C. Zhan and W. H. Ki, "Output-capacitor-free adaptively biased low-dropout regulator for System-on-Chips," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 5, pp. 1017-1028, May 2010.
- [8] C. Zhan and W. H. Ki, "A low dropout regulator for SoC with high power supply rejection and low quiescent current," in *Proc. IEEE 12th Int. Symp. Integr. Circuits*, Dec. 2009, pp. 37-40.
- [9] Y. H. Lam, W. H. Ki, and C. Y. Tsui, "Adaptively-biased capacitor-less CMOS low dropout regulator with direct current feedback," in *Proc. IEEE Asia South Pacific Conf. Des. Autom.*, Jan. 2006, pp. 104-105.
- [10] Bernard Friedland, "Control systems design : an introduction to state-space methods," 1st ed. New York: McGraw-Hill, 2005.